



Substitute for form 1449A/PTO				Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	09/966,224
				Filing Date	September 28, 2001
				First Named Inventor	Michael D. Ruehle
				Art Unit	2136
				Examiner Name	Carl G. Colin
				Attorney Docket Number	42390P11974
Sheet	1	of	2		

Examiner Signature	<i>Paul Cari</i>	Date Considered	3/21/06
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[Redacted] Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

**Applicant's unique citation designation number (optional). See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. *Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. Applicant is to place a check mark here if English language Translation is attached.*

Based on PTO/SB/08A (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wtr) 08/11/2003.

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Sheet **2** of **2***Complete if Known*

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CG		JYH-HUEI GUO ET AL., "A Novel Digit-Serial Systolic Array for Modular Multiplication", <i>Proceedings of the IEEE International Symposium on Circuits and Systems</i> , May 31-June 3, 1998, Monterey, California, pg. II-177-180.	
CG		JYH-HUEI GUO ET AL., "Design and Implementation of an RSA Public-Key Cryptosystem", <i>Proceedings of the IEEE International Symposium on Circuits and Systems</i> , 1999, pg. I-504-507.	
CG		C.D. WALTER, "Systolic Modular Multiplication", <i>IEEE Transactions on Computers</i> , Vol. 42, No. 3, March 1, 1993, pg. 376-378, IEEE Inc., New York, US.	
CG		WEIXIN GAI ET AL., "A Systolic Linear Array for Modular Multiplication", <i>Proceedings of the IEEE 2nd International Conference on ASIC</i> , October 1996, pg. 171-174.	

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